

Description

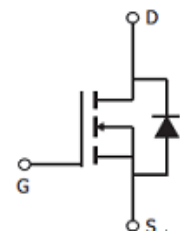
The G08N06S uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

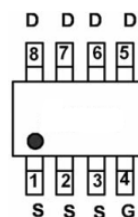
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- | V_{DSS} | $R_{DS(ON)}$
@ 10V (Typ) | $R_{DS(ON)}$
@ 4.5V (Typ) | I_D |
|-----------|-----------------------------|------------------------------|-------|
| 60V | 24 m Ω | 30 m Ω | 6A |
- High density cell design for ultra low R_{dson}
 - Fully characterized avalanche voltage and current
 - Good stability and uniformity with high E_{AS}
 - Excellent package for good heat dissipation
 - RoHS Compliant

Application

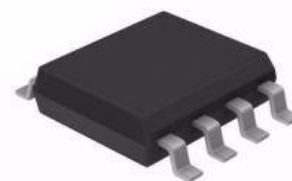
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



SOP-8 top view

Ordering Information

Part Number	Marking	Case	Packaging
G08N06S	G08N06	SOP-8	4000pcs/Reel

Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	6	A
Drain Current-Continuous($T_C=100^{\circ}\text{C}$)	$I_D (100^{\circ}\text{C})$	4.2	A
Pulsed Drain Current	I_{DM}	32	A
Maximum Power Dissipation	P_D	2	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	62.5	$^{\circ}\text{C/W}$
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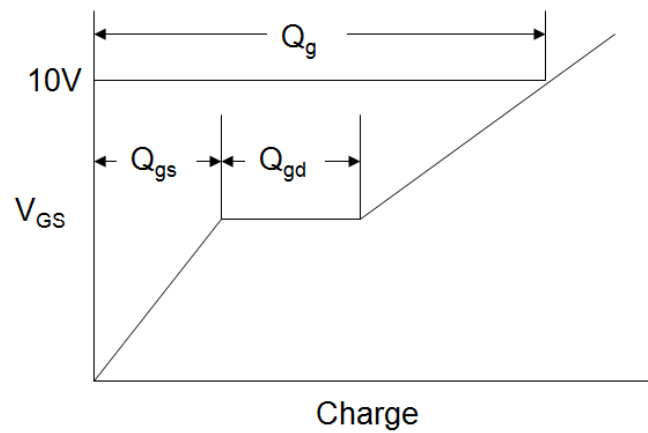
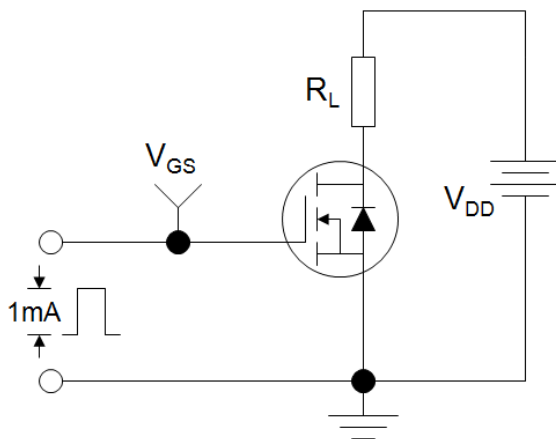
Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1	1.7	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =3A,	-	24	30	mΩ
	R _{DS(ON)}	V _{GS} =4.5V, I _D =3A,	-	30	40	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =3A	11	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =30V,V _{GS} =0V, F=1.0MHz	-	979	-	pF
Output Capacitance	C _{oss}		-	120	-	pF
Reverse Transfer Capacitance	C _{rss}		-	100	-	pF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, R _L =6.7Ω V _{GS} =10V,R _G =3Ω	-	5.2	-	nS
Turn-on Rise Time	t _r		-	3	-	nS
Turn-Off Delay Time	t _{d(off)}		-	17	-	nS
Turn-Off Fall Time	t _f		-	2.5	-	nS
Total Gate Charge	Q _g	V _{DS} =30V,I _D =5A, V _{GS} =10V	-	22	-	nC
Gate-Source Charge	Q _{gs}		-	3.3	-	nC
Gate-Drain Charge	Q _{gd}		-	5.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =3A,	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	5	A
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

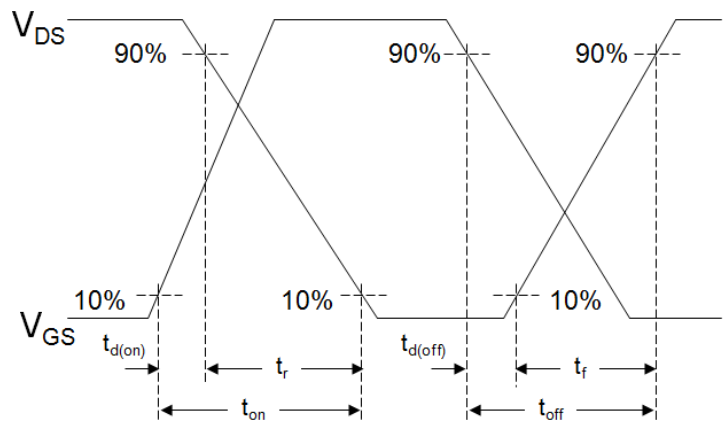
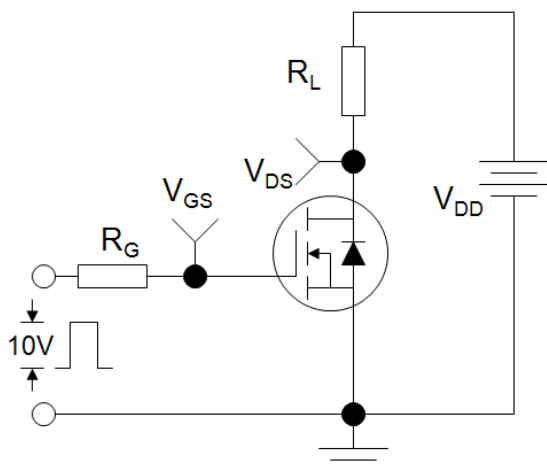
Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25\Omega$

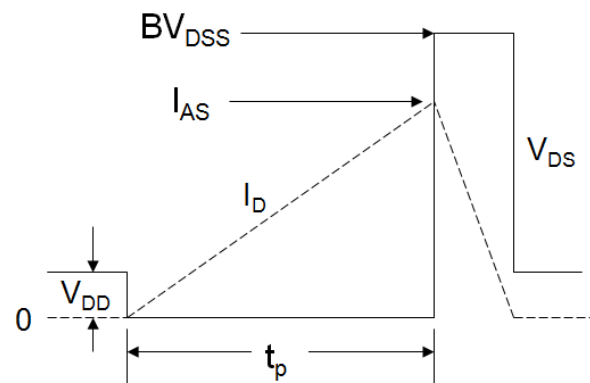
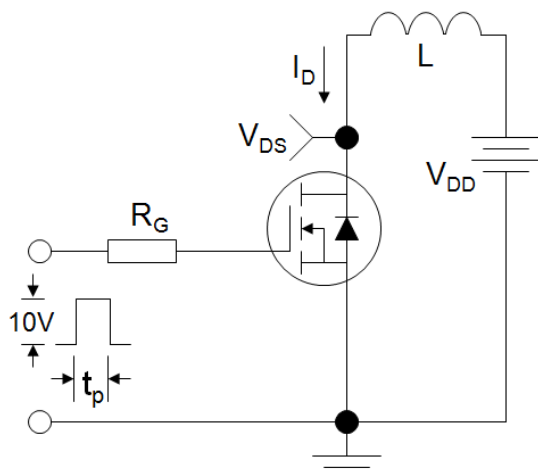
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

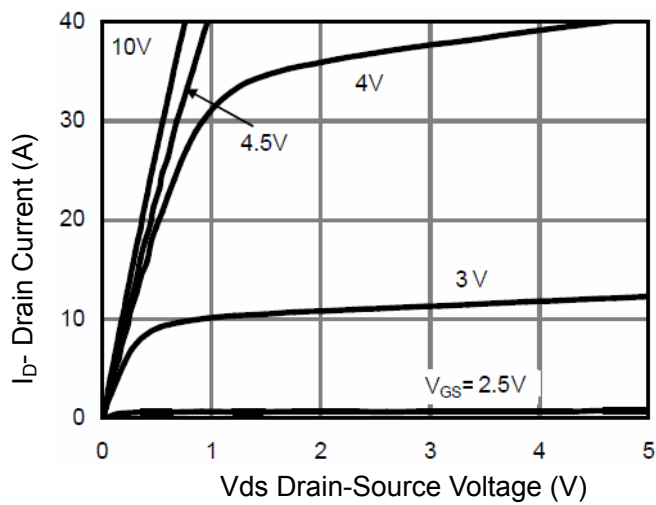


Figure 1 Output Characteristics

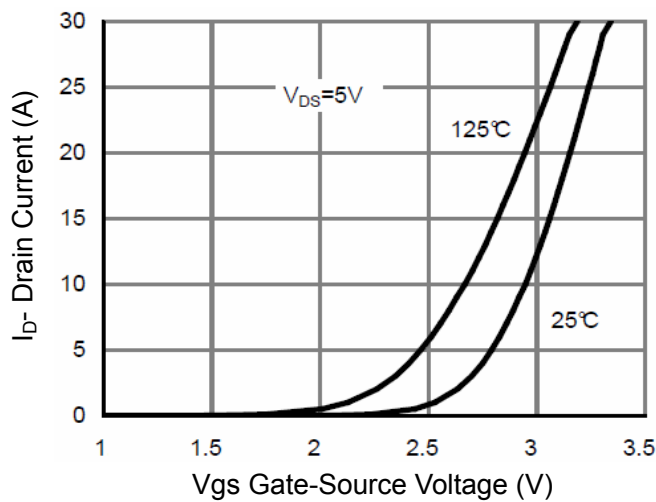


Figure 2 Transfer Characteristics

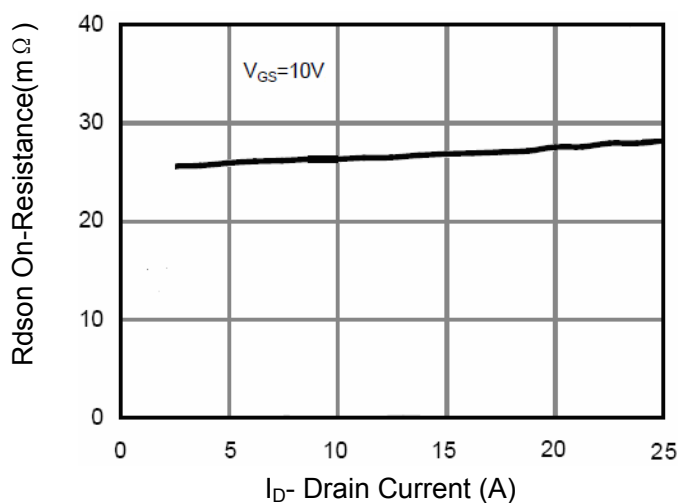


Figure 3 $R_{DS(on)}$ - Drain Current

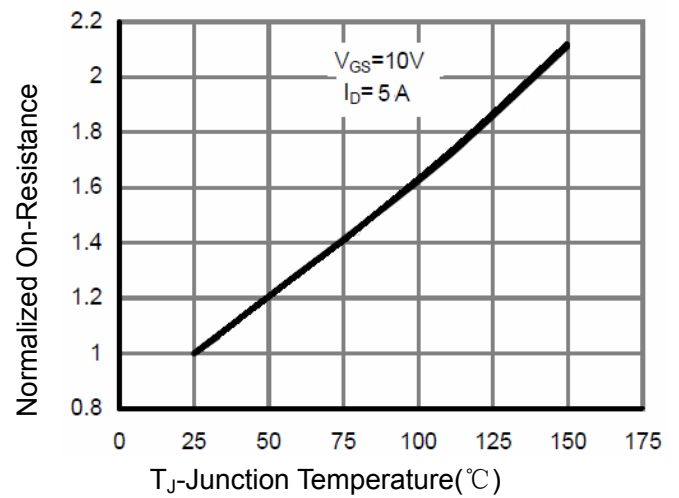


Figure 4 $R_{DS(on)}$ -Junction Temperature

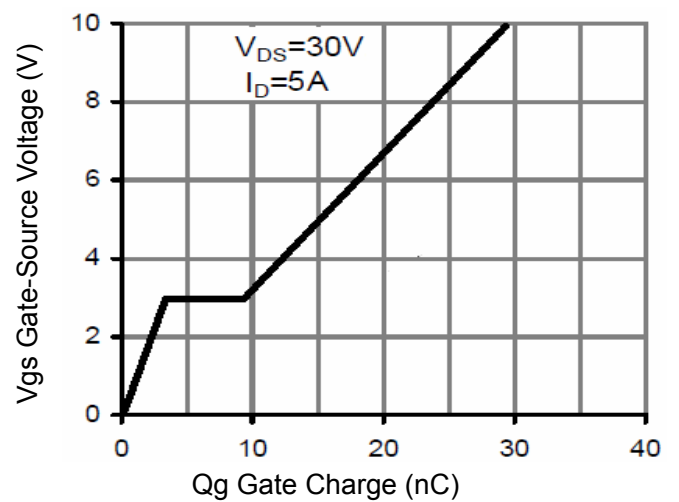


Figure 5 Gate Charge

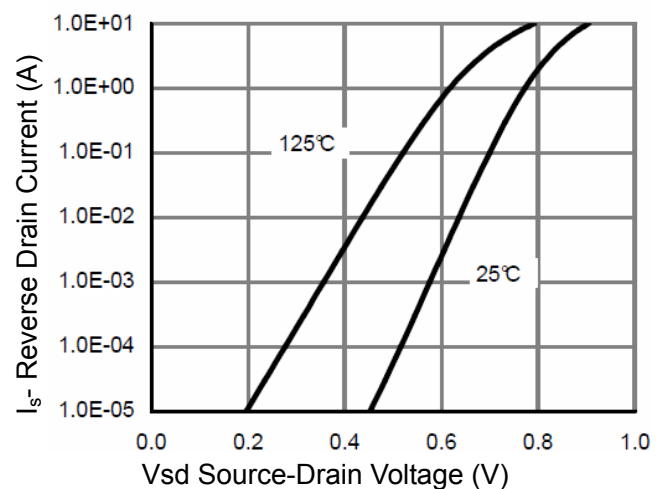


Figure 6 Source- Drain Diode Forward

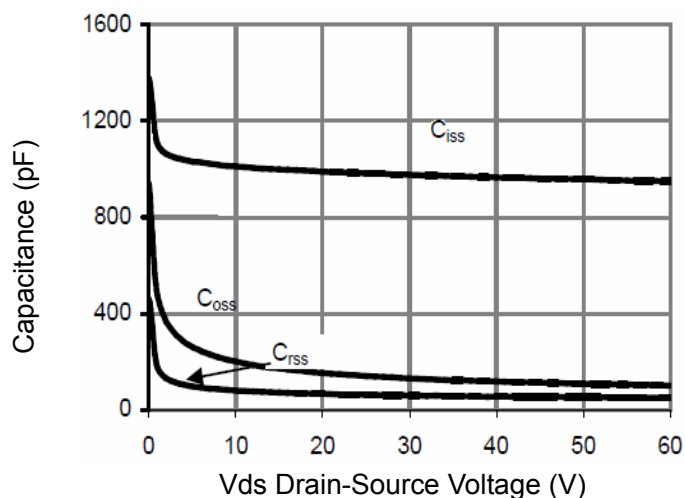


Figure 7 Capacitance vs Vds

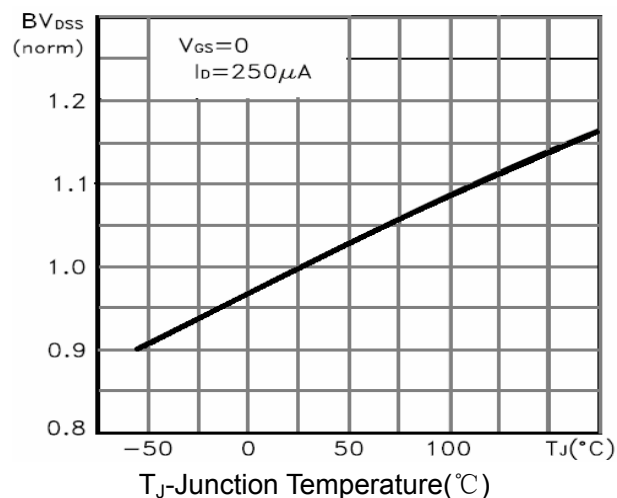


Figure 9 BV_{DSS} vs Junction Temperature

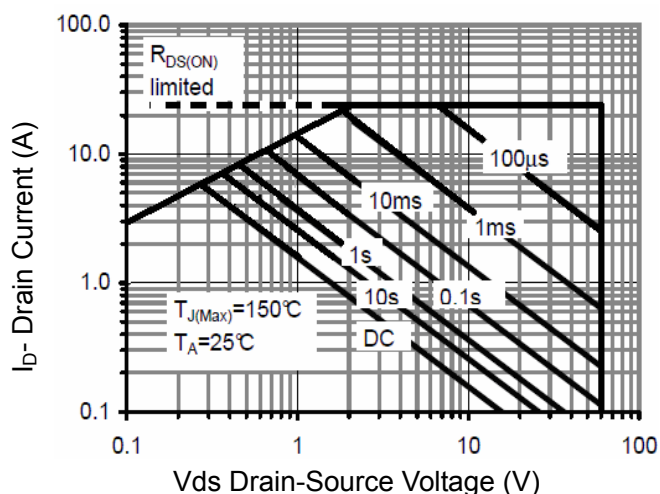


Figure 8 Safe Operation Area

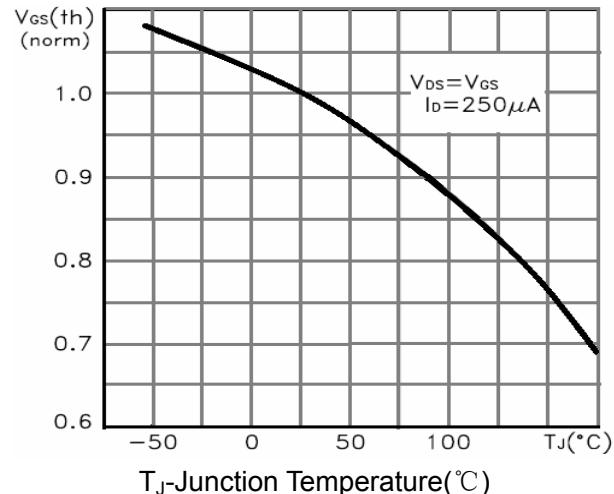


Figure 10 $V_{GS(th)}$ vs Junction Temperature

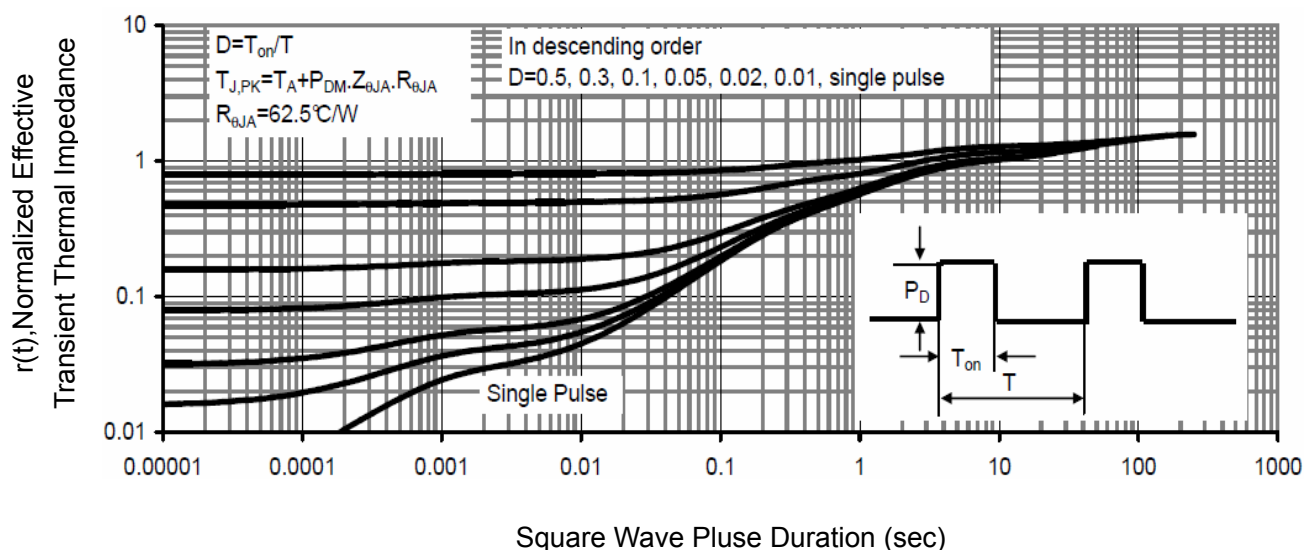
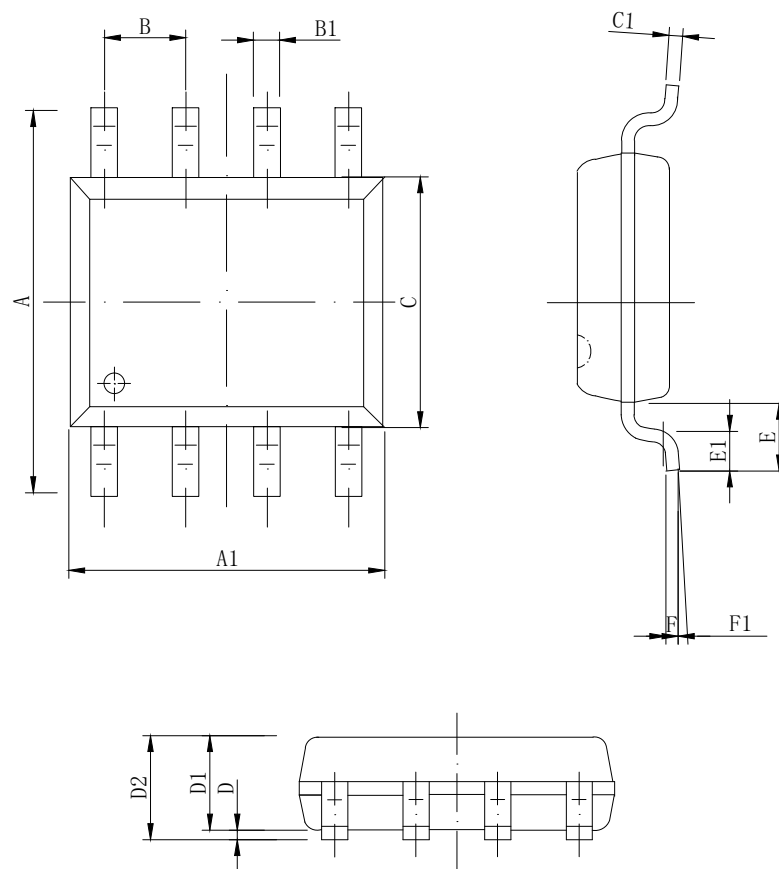


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package information



DIM	MIN	NOM	MAX
A	5.800	6.000	6.200
A1	4.800	4.900	5.000
B	1.270BSC		
B1	0.35 ^ 8x	0.40 ^ 8x	0.45 ^ 8x
C	3.780	3.880	3.980
C1	—	0.203	0.253
D	0.050	0.150	0.250
D1	1.350	1.450	1.550
D2	1.500	1.600	1.700
E	1.060 REF		
E1	0.400	0.700	0.100
F	0.250BSC		
F1	2°	4°	6°

All Dimensions in mm